REMARKS

Claims 1 – 11 are pending and under consideration in the above-identified application.

In the Office Action, Claims 1 – 3, 5, 7, and 9 – 11 were rejected, and Claims 4, 6, and 8 were objected.

In this Amendment, Claims 1 and 9 are amended. No new matter has been introduced as a result of this amendment.

Accordingly, Claims 1 – 11 remain at issue.

I. Objection To Claims

Claims 4, 6, and 8 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants respectfully traverse these claim objections as the corresponding rejected base Claim 1 is shown below to be patentable over the cited prior art to Kashima.

II. 35 U.S.C. § 102 Anticipation Rejection of Claims

Claims 1-3, 5, 7 and 9-11 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kashima et al. ("Kashima") (U.S. Publication No. 2002-0149558). Applicants respectfully traverse this rejection.

Claim 1 is directed to a display apparatus. The display apparatus comprises a pixel array unit, a clock generating unit, a shift register, a group of first switches, and a group of second switches. Claim 1 further recites that the start pulse has a pulse width that includes a plurality of pulse widths of the first clock pulses.

In one advantageous aspect of the start pulse width including a plurality of pulse widths of the first clock pulses, the pulse width of each of the transfer pulses for extracting each of the second pulses is increased in accordance with the pulse width of the horizontal start pulse. Therefore, a large margin can be obtained in the phase relationship between the second clock pulse and the transfer pulse.

In contrast, Kashima fails to teach or suggest that the start pulse has a pulse width that includes a plurality of pulse widths of the first clock pulses. In fact Kashima states in Paragraph [0003] that:

> "The shift register 101 is formed of n number of shift stages (transfer stages). When a horizontal start pulse HST is given, the shift register 101 performs a shift operation in synchronization with the opposite phase horizontal clocks HCK and HCKX. As a result, the shift stages of the shift register 101, as shown in the timing charts of FIGS. 2A to 2F, sequentially output the shift pulses Vs1 to Vsn having the same pulse width as the period of the horizontal clocks HCK and HCKX. These shift pulses Vs1 to Vsn are supplied to switches 102-1 to 102-n of the clock sampling switch group 102."

and further in Paragraph [0051] that:

> "Above for example the pixel part 15, a horizontal driving circuit (HDRV) 17 is disposed. Also, a clock generating circuit (CLKGEN: timing generator) 18 for supplying various clock signals to the vertical driving circuit 16 and the horizontal driving circuit 17 is provided. This clock generating circuit 18 generates a vertical start pulse VST for instructing the start of vertical scanning, opposite phase vertical clocks VCK and VCKX serving as a vertical scanning reference, a vertical start pulse VST for instructing the start of horizontal scanning, and opposite phase horizontal clocks HCK and HCKX serving as a horizontal scanning reference."

And still further in Paragraph [0055] that:

> "The shift register 21 is comprised by four shift stages (S/R stages) 21-1 to 21-4 corresponding to the pixel strings of the pixel part 15 (in the present example, four columns). When the horizontal start pulse HST is given, the shift register 21 performs a shift operation in synchronization with the opposite phase horizontal clocks HCK and HCKX. As a result, the shift stages 21-1 to 21-4 of the shift register 21, as shown in the timing charts of FIGS. 13A to 13M, output in sequence shift pulses Vs1 to Vs4 having the same pulse width as the period of the horizontal clocks HCK and HCKX."

Thus, based on at least the above cited paragraphs and FIGs. 2A and 13A Kashima fails to teach or suggest that the start pulse has a pulse width that includes a plurality of pulse widths of the first clock pulses.

Accordingly, Claim 1 is patentable over Kashima, as are dependent Claims 1-3, 5, and 7 for at least the same reasons.

Claim 9 recites the same distinguishable limitation as Claim 1. Thus, Claim 9 is patentable over Kashima, as are dependent Claims 10 and 11 for at least the same reasons.

III. Conclusion

In view of the above amendments and remarks, Applicant submits that Claims 1 – 11 are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

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